A Comparative Analysis of Vernier Delay Line TDC based on Resolution, Area, Power and Conversion Time

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Abstract: Time to Digital Converters (TDC) are devices used to identify an event. TDCs can also be used to measure time interval between two events. One of the key components of All Digital Phase Locked Loop (ADPLL) is TDC. ADPLLs are used in applications such as Bluetooth, Wi-Fi and GSM. An attempt is made to compare Vernier Delay Line (VDL) TDC using Symmetric SR Latch, VDL TDC using Simplified SR Latch and VDL TDC using Simplified Sampler. The results are compared on the basis of Resolution, Area, Power and Conversion Time. The VDL TDC architectures having 19 stages are implemented in Cadence virtuoso gpdk 45 nm technology with a supply voltage of 1.2 V. All the implemented VDL architectures produce a same resolution of 2 ps at 1 GHz input frequency. VDL TDC using Symmetric SR Latch consumes 722 transistors, 5.792 mW of power and 1.0175 ns of conversion time. VDL TDC using Simplified SR Latch consumes 570 transistors, 3.385 mW of power and 1.0609 ns of conversion time. Similarly, VDL TDC using Simplified Sampler consumes 532 transistors, 4.929 mW of power and 497.4 ps of conversion time. The simulation results show that VDL TDC using Simplified Sampler is more efficient in terms of area and conversion time.

Keywords: Time to Digital Converter (TDC), All Digital Phase Locked Loop (ADPLL), Vernier Delay Line (VDL).

Introduction

A TDC is a device that quantizes time interval between two rising edges. A TDC has application in laser range finder, phase meters, space science instruments, physical instruments and measurement devices. There are several advantages of digital methods over analog methods. The digital methods are immune to external disturbances, have ease of implementation in integrated circuit, shorter conversion time and they are flexible. Digital methods are efficient to design and have high productivity. The PLL is a negative feedback control system in which one signal chases the other signal. The traditional charge pump based PLL is made up of analog devices, while ADPLL is made up of digital devices. Currently, TDCs are used as phase detectors in ADPLL. Fig. 1 shows the block diagram of ADPLL where the Phase error between reference and clock signal is detected by TDC.

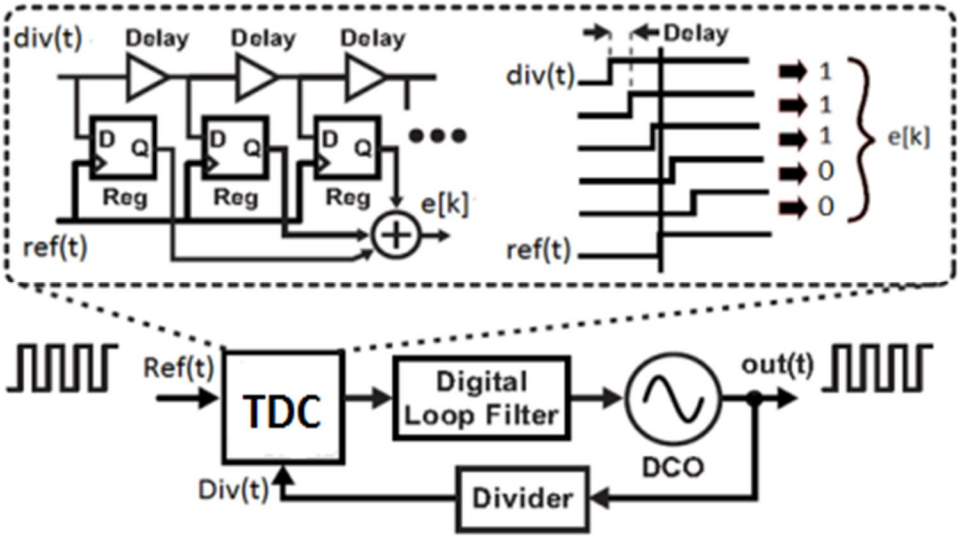

Fig. 1: TDC in All Digital Phase Locked Loop [9]

There are numerous TDC architectures. Most basic TDC architecture is Flash type TDC. It has a simple structure, very easy to implement, consumes very less area and hence less power. It does not provide good resolution compared to other architecture. VDL TDC has better resolution compared to all. On the contrary, it consumes more area and hence becomes impractical. To overcome the problem of area consumption, Vernier ring TDC is proposed. It has a ring structure and hence consumes less area. VDL TDC is limited by mismatch between devices. Replica delay line type TDC makes use of additional set of inputs for overcoming the problem of mismatch between devices. Replacing buffers by inverters improves resolution of TDC.

An attempt is made to compare VDL TDC using Symmetric SR Latch with VDL TDC using Simplified SR Latch based on Resolution, Area, Power and Conversion Time.

Literature Survey

PiotrDudek, Stanislaw Szczepan ´ski and John, V. Hatfield, designed a CMOS TDC integrated circuit utilizing tapped delay lines that achieves high resolution with low dead-time [1]. Win Chaivipas, Akira Matsuzawa, and Philipus Chandra Oh compared ADPLL with the traditional charge pump based Phase Locked Loop (PLL). The paper lists some of its advantages, which are used to improve the system's performance [2]. An ADC based on digital delay lines is designed by Guansheng Li, Yahya, M. Tousi, ArjangHassibi and EhsanAfshari and the effects of jitter and mismatch is studied. It is established that the ADC becomes more power efficient with scaling [3]. Jianjun Yu, Fa Foster Dai, Fellow, Richard C. Jaeger and Life Fellow presented a novel Vernier ring TDC that places the Vernier delay cells and arbiters in a ring format. The proposed TDC thus achieves large detectable range, fine time resolution, small die size and low power consumption simultaneously [4]. A high resolution TDCs and layout for the same is realized by Mismatch between devices are analyzed by Chen Yo, Dr. Fredrik Jonsson and Dr. Jian Chen. [5]. Ping Lu, Antonio Liscidini and PietroAndreani designed and implemented two Gated Ring Oscillator's (GRO) that act as the delay lines in improved Vernier TDC and showed the improvement of the trade-off between time resolution, conversion speed and absolute delay. The proposed TDC is well suited for use in a high-speed Digital PLL [6]. A comparison of various TDCs, on the basis of Resolution, Range and Area has been conducted. Tests were conducted on Buffer delay line based TDC, Inverter chain based TDC and VDL based TDC by Kashyap Vijaya and Porwal Saurabh [7]. In 2015 the performance of various types of TDCs were compared. It has been concluded that VDL TDC has better resolution than rest of the TDC architecture but consumes very large area which limits its practical application by C.Priyanka and P.Latha [8].

Compared to flash TDC, VDL TDC provides a better resolution. However VDL TDC consumes large amount of area, power and also its delay cells need to be matched. So there is scope for reducing area and power. In this context an attempt is made to reduce the area and power requirements.

Vernier Delay Line TDC

Basic layout of VDL TDC is shown in Fig. 2. TDC is made up of delay elements and sampling elements. The number of stages N required for the TDC is calculated as shown by (1).

$$N = \frac{\Delta T}{Tlsb} \quad (1)$$

ΔT represents the measurement time interval and Tlsb is the effective time resolution. The effective time resolution (Tlsb) is calculated as shown by (2).

$$T_{lsb} = Γ1 - Γ2 \quad (2)$$

Γ1 is the delay offered by upper buffer chain and Γ2 is the delay offered by lower buffer chain. The time interval ΔT is calculated as shown by (3).

$$\Delta T = N\, T_{lsb} + Ɛ \quad (3)$$

Ɛ is the quantization error. Fig. 3 shows the signal propagation in VDL TDC. The measurement time interval is the difference between the start and stop signal. The delay Γ1 offered by the buffer in the upper chain is greater than the delay Γ2 of buffer in the lower chain (Γ1 > Γ2). The time difference between START and STOP (Γ1- Γ2) signal reduces as START and STOP signal propagates in their respective delay chain. The position in the delay chain where the STOP signal catches up with the START signal is the measured time.

The output is a word that describes the evaluated time. It is encoded as a position of HIGH/LOW transitions. Very small resolution can be achieved as resolution is equal to the difference of delays between two chains of buffer. Hence it is possible to achieve any resolution with VDL TDC architecture.

Array of delay lines and pulse shrinking delay line can also be used to improve the resolution of delay line. To achieve a remarkable improvement in the resolution using array of delay line, it is necessary to build very large arrays. Dynamic range is limited in this case. There is deep rooted burden of long dead time in pulse shrinking delay line. This makes it unsuitable for applications where large number of STOP signal gets generated. These limitations are absent in VDL TDC.

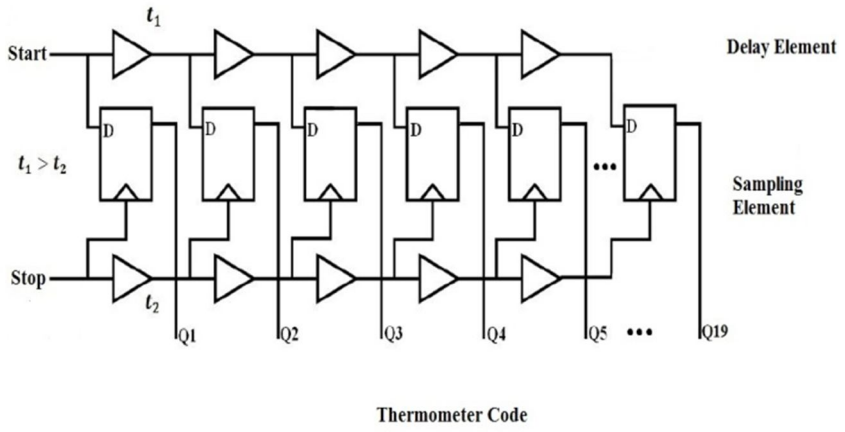

Fig. 2: Vernier Delay Line TDC Architecture [9]

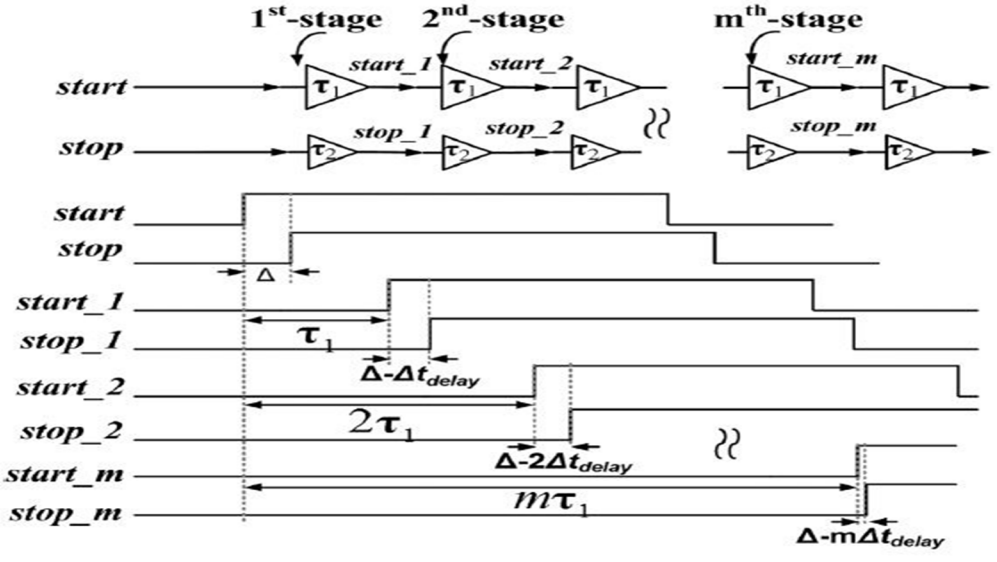

Fig. 3: Signal propagation in a VDL TDC [6]

Delay Element

Delay elements are implemented as simple buffers as shown in Fig. 4. It consists of two inverters in series. The delay depends greatly on width of transistors and hence current through the MOS transistor. As width of the transistor increases, delay increases. The matching of buffer delays determines the accuracy of TDC conversion. Therefore mismatch between the MOS transistors limits the accuracy of the TDC. The problem of mismatch between MOS transistor can be tackled by using large transistors. This increases the consumption area and in turn increases power consumption.

Sampling Element

Samplers are constructed using Sense Amplifier and SR Latch. Fig. 5 shows the block diagram of Sampling Element.
The circuit diagram of Sampler used by Cheng Yo [5] is shown in Fig. 6.
Sense Amplifiers senses the complementary differential inputs. After sensing the differential inputs, monotonous transition from HIGH to LOW is produced in one of the outputs. When clock is LOW, $\overline{S}$ and $\overline{R}$ are charged to HIGH since there is no path to ground. When Clock is HIGH and if D is HIGH, $\overline{S}$ gets discharged to ground, while $\overline{R}$ retains its charge. When clock is HIGH and if $\overline{D}$ is HIGH, $\overline{R}$ gets discharged to ground, while $\overline{S}$ retains its charge. The size of input transistor should be large enough to ensure the speed, but should be small enough to minimize the load effect of Sense Amplifier. Sizes of transistors are adjusted and both PMOS and NMOS networks are matched to have equal delay. SR Latch holds the output of the Sense Amplifier until next leading clock edge. Symmetric SR Latch ensures the equal delay from clock to Q and clock to $\overline{Q}$. Hence clock skew is minimized. Next state of Q and $\overline{Q}$ can be calculated as shown by (4) and (5).

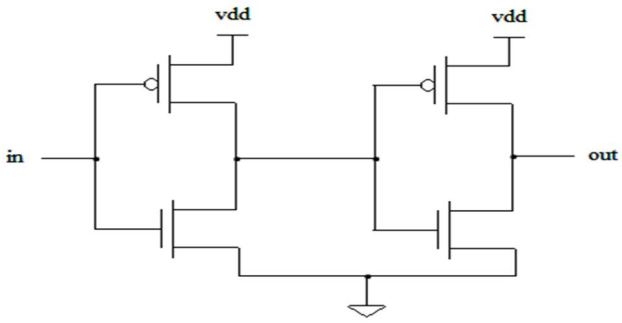

Fig. 4: Circuit diagram of Delay Element

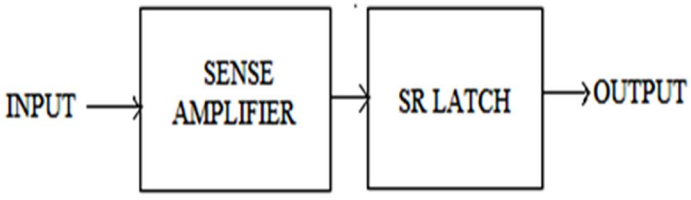

Fig. 5: Block diagram of Sampling Element

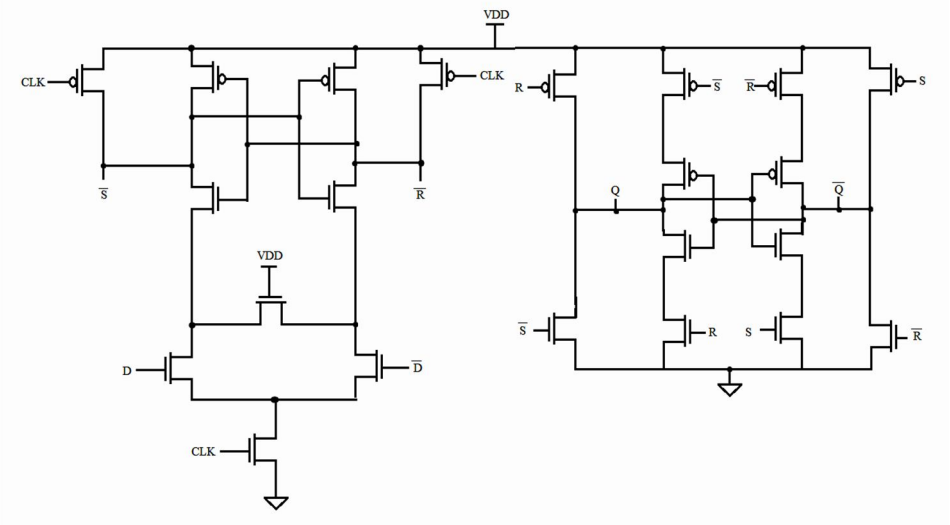

Fig. 6: Circuit diagram of Sampler using Symmetric SR Latch

$$Q^{+} = S + \overline{R}\,.Q \tag{4}$$

$$\overline{Q}^{+} = R + \overline{S}\,.\,\overline{Q} \tag{5}$$

However cross coupled NAND SR Latch has a simpler structure and consumes less number of transistors compared to Symmetric SR Latch. Hence Symmetric SR Latch is replaced by cross coupled NAND SR Latch (Fig.7) by retaining the Sense Amplifier. It is observed that power consumption of the circuit is greatly reduced. Thus the next state of Q and $\overline{Q}$ is given by (6) and (7).

$$Q^{+} = S + Q \tag{6}$$

$$\overline{Q}^{+} = R + \overline{Q} \tag{7}$$

The circuit is further simplified by replacing the Sense Amplifier with a simplified structure [7] as shown in Fig. 8. SR Latch is implemented as cross coupled NAND structure. When clock is LOW, irrespective of the state of D and $\overline{D}$, both $\overline{S}$ and $\overline{R}$ are charge to HIGH. When clock and D are HIGH, $\overline{S}$ gets discharged. When clock and $\overline{D}$ is HIGH, $\overline{R}$ get discharged. Next state

of Q and $\overline{Q}$ is given by (6) and (7). It is observed that transistor count and conversion time of the Sampler is further reduced for the same resolution.

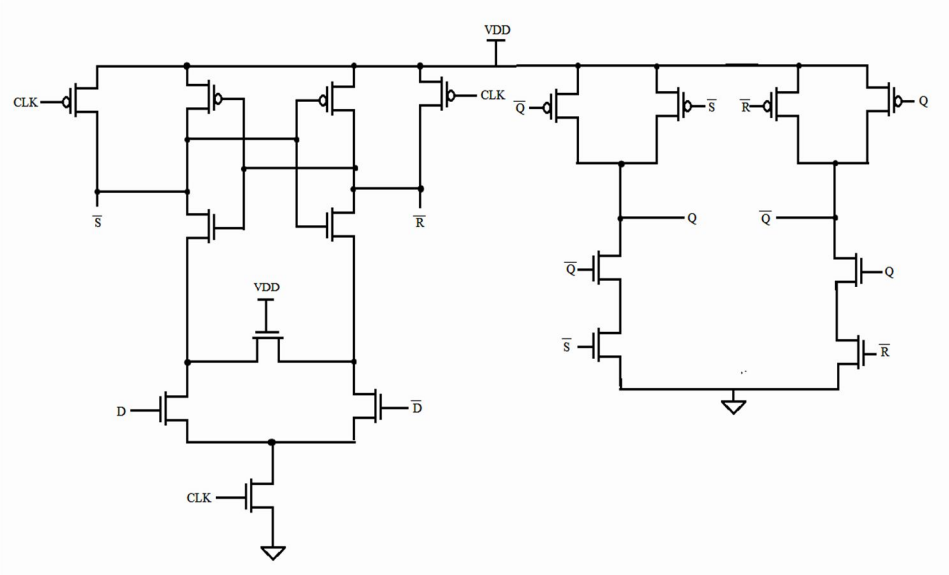

Fig. 7: Circuit diagram of Sampler using Simplified SR Latch

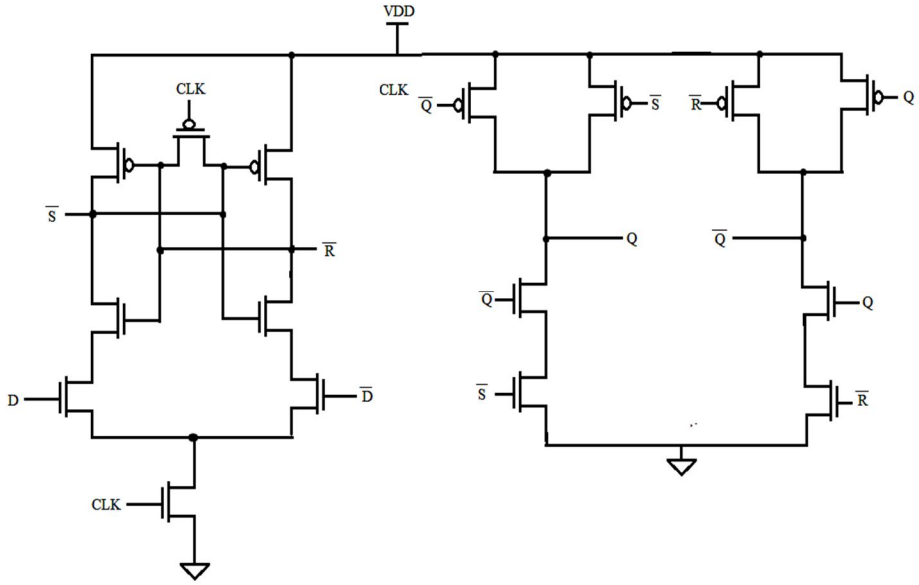

Fig. 8: Circuit diagram of Simplified Sampler

Simulation Results

The study presents the comparison between VDL TDC using Symmetric SR Latch, VDL TDC using Simplified SR Latch and VDL TDC using Simplified Sampler. This VDL implementation contains delay line of 19 stages. Fig. 9 and Fig. 10 show the output of VDL TDC using Symmetric SR Latch. Fig. 11 shows the plot of power versus time of VDL TDC using Symmetric SR Latch. Fig. 12 and Fig. 13 show the output of VDL TDC using Simplified SR Latch. Fig. 14 shows the plot of power versus time of VDL TDC using Simplified SR Latch. Fig. 15 and Fig. 16 show the output of VDL TDC using Simplified Sampler. The VDL TDC is implemented using gpdk 45 nm technology with a supply voltage of 1.2 V. All the three VDL TDCs have a resolution of 2 ps operating at a frequency of 1 GHz. The VDL TDC using Symmetric SR Latch has transistor count of 722. This VDL TDC consumes 5.792 mW of power and has a conversion time of 1.0175 ns. The VDL TDC using Simplified SR Latch has transistor count of 570, has a power consumption of 3.385 mW and a conversion time of 1.0609 ns. The VDL TDC using Simplified Sampler has a transistor count of 532. It consumes 4.929 mW of power and has a conversion time of 497.4 ps.

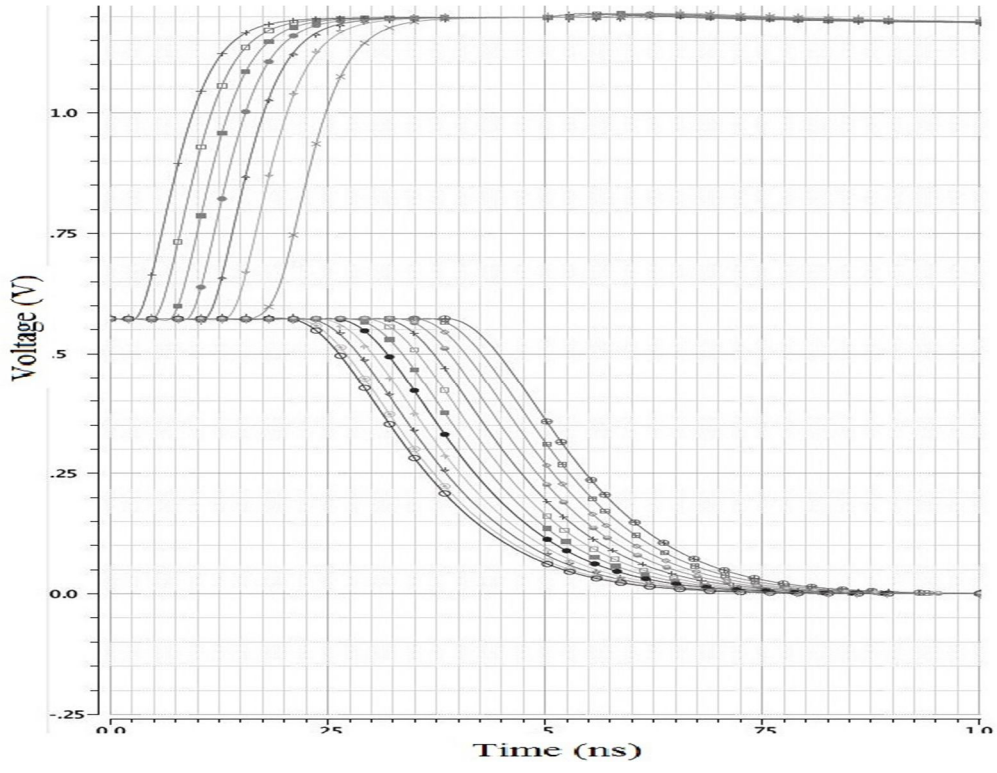

Fig. 9: Output of VDL TDC using Symmetric SR Latch for delay difference of 0 ps between start and stop signal

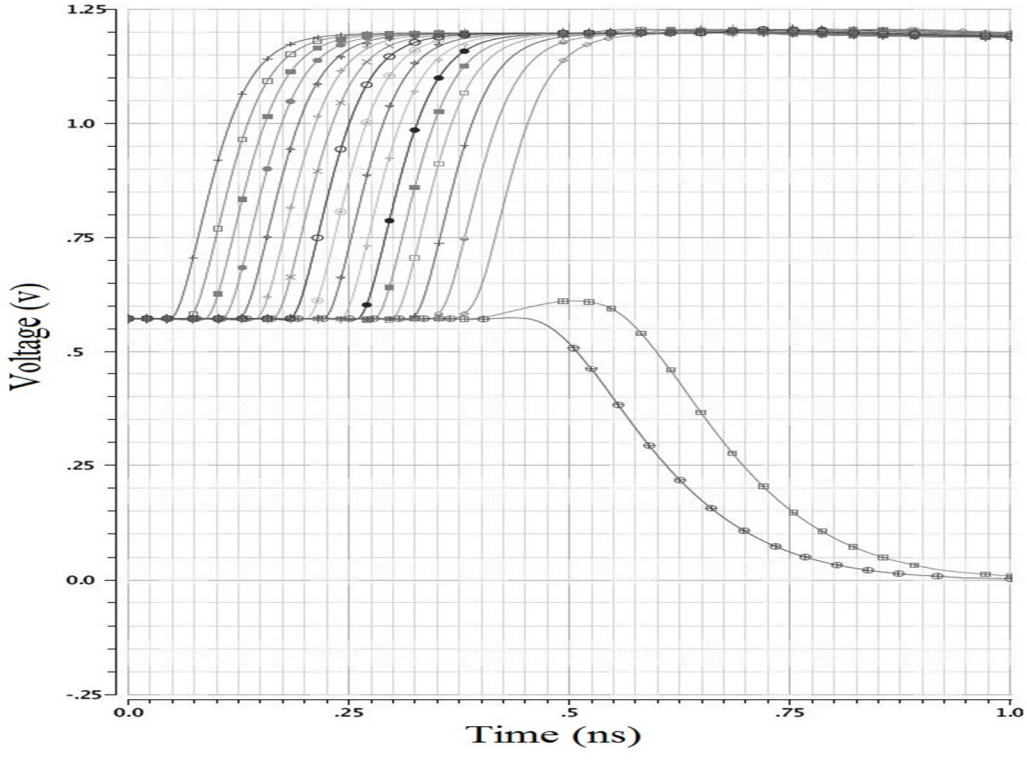

Fig. 10: Output of VDL TDC using Symmetric SR Latch for delay difference of 20 ps between start and stop signal

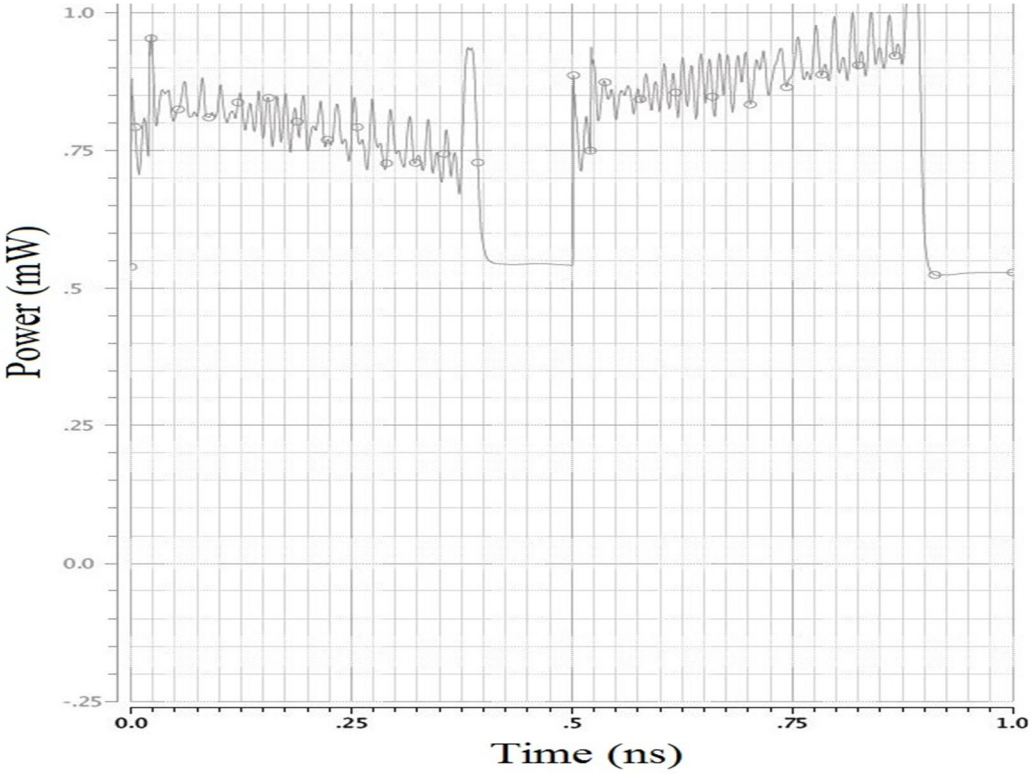

Fig. 11: Plot of Power vs Time for VDL TDC using Symmetric SR Latch

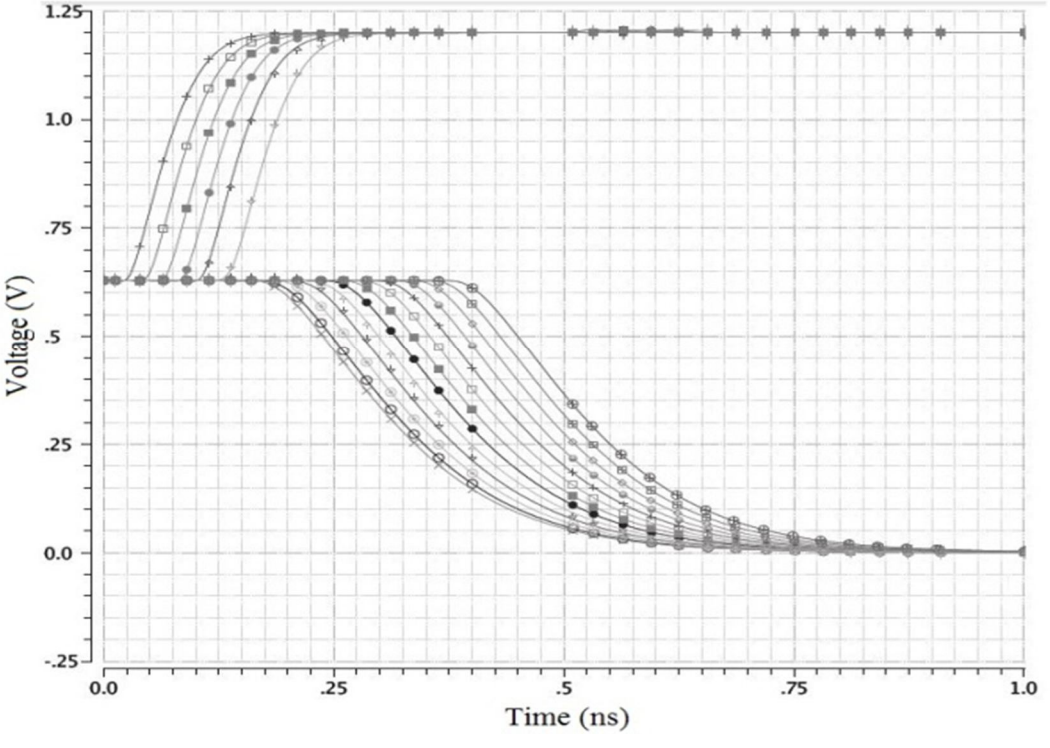

Fig. 12: Output of VDL TDC using Simplified SR Latch for delay difference of 0 ps between start and stop signal

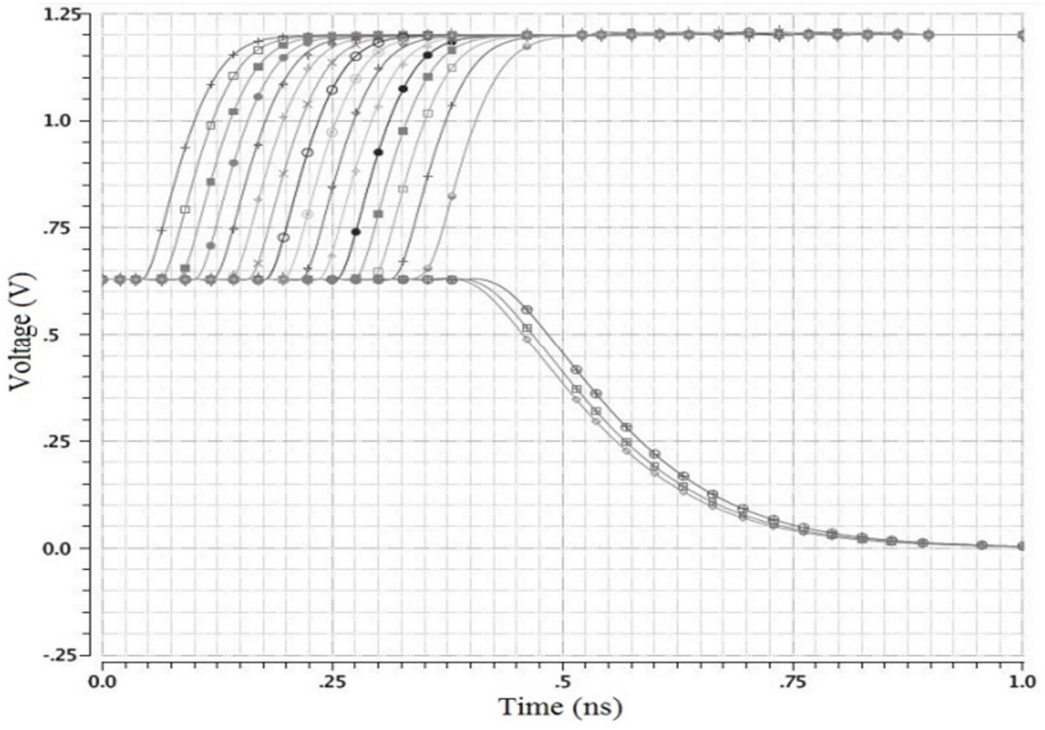

Fig. 13: Output of VDL TDC using Simplified SR Latch for delay difference of 20 ps between start and stop signal

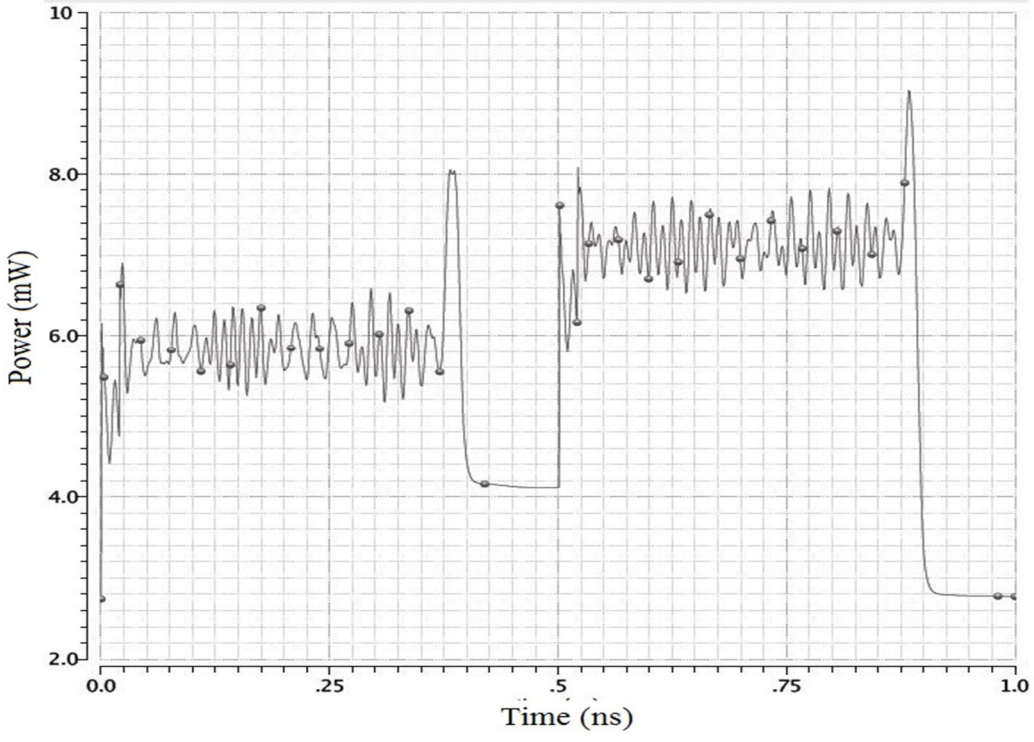

Fig. 14: Plot of Power vs Time for VDL TDC using Simplified SR Latch

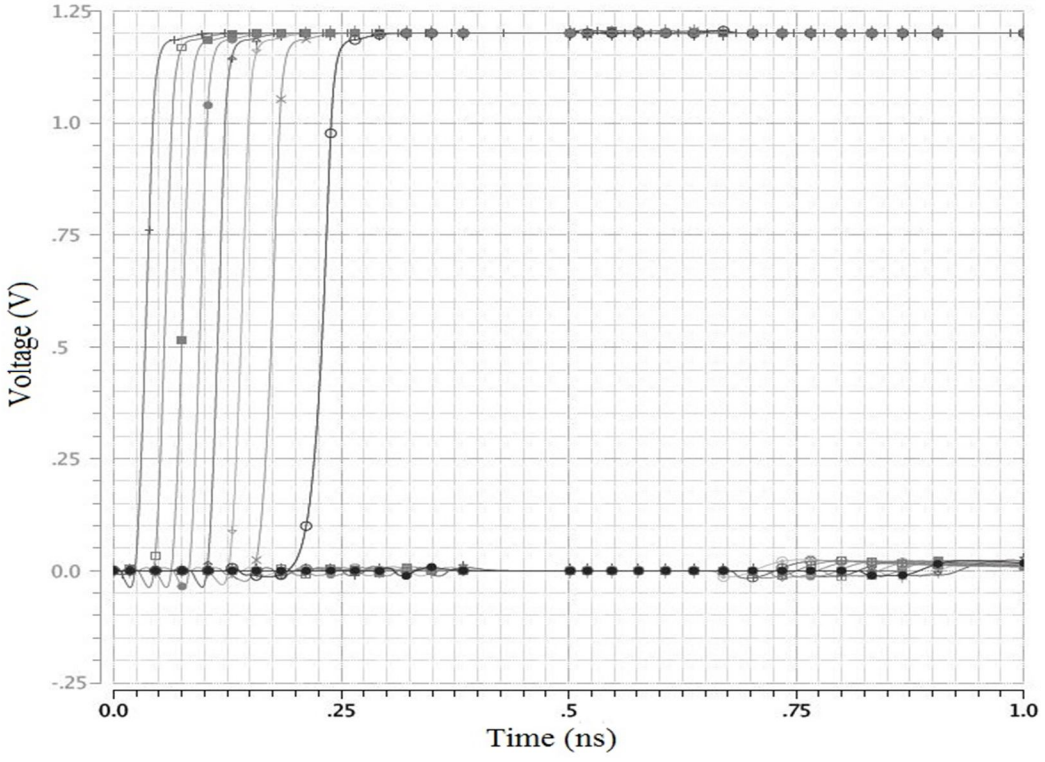

Fig. 15: Output of VDL TDC using Simplified Sampler for delay difference of 0 ps between start and stop signal

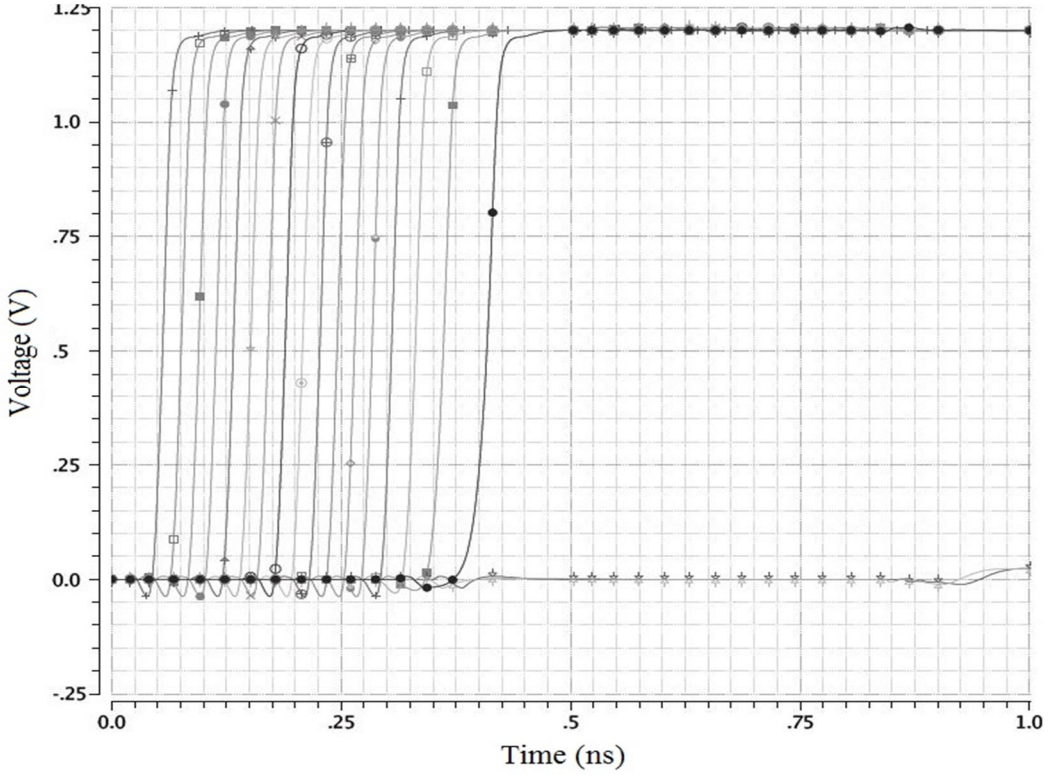

Fig. 16: Output of VDL TDC using Simplified Sampler for delay difference of 20 ps between start and stop signal

Table 1. Comparison of VDL TDC Architectures

Parameters	VDL TDC using Symmetric SR Latch [5]	VDL TDC using Simplified SR Latch	VDL TDC using Simplified Sampler
Supply voltage	1.2 V	1.2 V	1.2 V
Technology	gpdk 45 nm	gpdk 45 nm	gpdk 45 nm
Operating frequency	1 GHz	1 GHz	1 GHz
Resolution	2 ps	2 ps	2 ps
Transistor count	722	570	532
Power consumption	5.792 mW	3.385 mW	4.929 mW
Conversion Time	1.0175 ns	1.0609 ns	497.4 ps

Conclusion

Here, VDL TDC using Symmetric SR Latch, VDL TDC using Simplified SR Latch and VDL TDC using Simplified Sampler are analysed and the results are compared. The VDL TDC architectures are implemented using gpdk 45 nm technology for a supply voltage of 1.2 V in Cadence environment. Transistor count of VDL TDC using Simplified Sampler is less than VDL TDC using Symmetric SR Latch and VDL TDC using Simplified SR Latch by 190 and 38 respectively. Power consumed by VDL TDC using Simplified SR Latch is 2.407 mW lower than the VDL TDC using Symmetric SR Latch and is 1.544 mW lower than the VDL TDC using Simplified Sampler. Conversion time of VDL TDC using Simplified Sampler is 520.1 ps less than VDL TDC using Symmetric SR Latch and is 563.5 ps less than VDL TDC using Simplified SR Latch. Since all the implementations produce a resolution of 2 ps, VDL TDC using Simplified Sampler is found to be more efficient in terms of area and conversion time. In terms of power consumption, VDL TDC using Simplified SR Latch is found to be efficient.

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